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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/554,067	10/21/2005	Rebha El-Farhane	FR030044US1	8293
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NXP, B.V. NXP INTELLECTUAL PROPERTY DEPARTMENT M/S41-SJ 1109 MCKAY DRIVE SAN JOSE, CA 95131			EXAMINER CHHAYA, SWAPNEEL	
			ART UNIT 2822	PAPER NUMBER
			NOTIFICATION DATE 10/11/2007	DELIVERY MODE ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary

Application No.

10/554,067

Applicant(s)

EL-FARHANE, REBHA

Examiner

Swapneel Chhaya

Art Unit

2822

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 21 October 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-10 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-10 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 21 October 2005 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date 12/19/2005.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 7 objected to because of the following informalities:

Regarding part a of claim 7, it states "substrate in a first semiconductor material" is grammatically incorrect. Also, part f states "a portion in a second semiconductor material" is grammatically incorrect.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 7 and 10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding part d of claim 7, it is unclear what two surface films the claim is referring to.

For the purposes of this examination, this is being interpreted as two surface portions of the substrate are removed.

Regarding part e of claim 7 it is unclear as to what "said two electrode parts of the surface of the substrate" is referring to.

For the purposes of this examination, this is being interpreted as two electrode portions of the substrate are removed.

Art Unit: 2822

Regarding claim 10, it is known that a dependent claim inherits the limitations of the independent claim. Claim 7 states that the steps are done in a successive order, whereas claim 10 contradicts claim 7 and states that step e is performed before step d, which is not in successive order as previously claimed.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-3, 6 are rejected under 35 U.S.C. 102(b) as being anticipated by Wieczorek et al. (U.S. Patent 6274894).

Regarding claim 1. A semiconductor device comprising:
a gate electrode (44) (Fig. 10 column 9 lines 40-45) and
a gate insulating layer (42) produced on a part of the surface of a substrate (40) of a first semiconductor material having a given melting point, and surrounded by an

Art Unit: 2822

insulating spacer (50) in a plane parallel to the surface of the substrate, (Fig. 10 column 9 lines 26-35 column 10 lines 35-45)

the gate insulating layer being disposed between the substrate and the gate electrode (Fig. 10)

a source region and a drain region (60) situated under the surface of the substrate at the level of two opposite sides of the gate electrode respectively, each region containing electrical carriers of the same given type, with respective first concentrations, and each region comprising a portion of a second semiconductor material (56) disposed on the substrate below the level of the gate insulating layer in a direction perpendicular to the surface of the substrate, (Fig. 10 column 13 lines 20-45)

each portion of second material extending at least partially between the substrate and the spacer, substantially as far as a limit coming in line, in said perpendicular direction, with one side of the gate electrode (Fig. 10)

said portions of second material being doped with doping elements in order to create electrical carriers of said given type with second concentrations less than said first concentrations (Fig. 10 column 13 lines 20-45), and

said portions of second material having a melting point lower than the melting point of the first material, please note that this is inherent due to the materials used, namely the materials claimed in claim 3.

Regarding claim 2. A device as claimed in Claim 1, in which said portions of second material have an ability to absorb a light radiation greater than the absorption ability of

Art Unit: 2822

the first material for the same light radiation, please note that this is inherent in the reference due to the materials used, namely the materials claimed in claim 3.

Regarding claim 3. A device as claimed in Claim 1, in which the first material is based on silicon and the second material is based on germanium or based on an alloy of silicon and germanium (column 9 lines 15-25, column 12 lines 15-25)

Regarding claim 6. A device as claimed in claim 1, characterized in that said device is an MOS transistor (column 7 lines 50-60).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 4, 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wieczorek in view of Chau et al. (U.S. Patent 5710450).

Regarding claim 4. Wieczorek discloses the claimed invention except for the encapsulation portions disclosed on top of the portions of second material.

Chau discloses:

Art Unit: 2822

A device as claimed in Claim 1, also comprising two encapsulation (420) portions of said second material, disposed respectively over the portions of second material (314) on a side opposite to the substrate. (Fig. 4 column 6 lines 1-10, column 7 lines 50-60 column 8 lines 1-10)

It would have been obvious to one having ordinary skill in the art at the time the invention was made to implement the encapsulation portions as taught by Chau, since Chau states at column 7 lines 60-67 column 8 line 1-2 that such a modification would facilitate an adequate source/drain contact region for the fabricated device.

Regarding claim 5. Chau discloses:

A device as claimed in Claim 4, in which each encapsulation portion extends between the spacer and the portion of second material above which said encapsulation portion is disposed, substantially as far as a limit situated in line, in said direction perpendicular to the surface of the substrate, with the side of the gate electrode corresponding to said second encapsulation portion. (Fig. 4 column 6 lines 1-10, column 7 lines 50-60 column 8 lines 1-10)

5. Claims 7, 8, 9, and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chau et al. (U.S. Patent 5710450) in view of Andideh et al. (U.S. Patent 6121100) and further in view of Wieczorek et al. (U.S. Patent 6274894).

Art Unit: 2822

Regarding claim 7. Chau discloses:

A method of manufacturing a semiconductor device, comprising the following successive steps:

- a) a gate insulating layer (302) is formed on a part of a surface of a substrate (300) in a first semiconductor material having a given melting point (Fig. 3A column 4 lines 25-30)
- b) a gate electrode (306) is formed on top of the gate insulating layer (Fig. 3A column 4 lines 30-35)
- c) an insulating spacer (308) is formed, disposed around the gate insulating layer and the gate electrode, parallel to the surface of the substrate (Fig. 3A-3F column 4 lines 45-65)
- d) two surface films of the first material are removed respectively in two lateral parts of the surface of the substrate situated on two opposite sides of the surface part of the substrate carrying the gate insulating layer and the gate electrode, each lateral part extending between the substrate and the spacer substantially as far as a limit coming in line with one of the opposite sides of the gate electrode in a direction perpendicular to the surface of the substrate (Fig. 3A-3F column 4 lines 60-67, column 5 lines 1-5)

Chau discloses the claimed invention except for the formation of the deep source/drain regions prior to the formation of the extensions.

Andideh teaches:

Art Unit: 2822

e) a source region and a drain region (310) are formed, each region being situated below the surface of the substrate at a level of said two electrode parts of the surface of the substrate respectively, each region containing electrical carriers of the same given type with respective first concentrations; (Fig. 3F column 8 lines 50-60)

f) there is formed on the substrate, in each lateral part a portion in a second semiconductor material (318) substantially as far as a limit coming in line, in said perpendicular direction, with the opposite side of the gate electrode corresponding to said lateral part, said portions of second material containing doping elements in order to create electrical carriers of the given type, and having a melting point lower than the melting point of the first material; (Fig. 3F-3h column 8 lines 20-65)

It would have been obvious to one having ordinary skill in the art at the time the invention was made to form the deep source/drain implants prior to the formation of the source/drain extensions as taught by Andideh, since Andideh states at column 8 line 603-67 column 9 lines 1-5 that such a modification would enable a deeper implant using relatively low energy.

Chau in view of Andideh discloses the claimed invention except for the heating of the portions of the second material.

Wieczorek discloses:

g) the portions of second material are heated to a temperature intermediate between the respective melting points of the first and second materials,

Art Unit: 2822

so that the portions of second material contain electrical carriers with second concentrations lower than said first concentrations. (column 13 lines 20-45)

It would have been obvious to one having ordinary skill in the art at the time the invention was made to heat the portions of the material as taught by Wieczorek, since Wieczorek states at column 13 line 35-45 that such a modification would activate the impurities and repair damage to the substrate.

Regarding claim 8.

Chau in view of Andideh and further in view of Wieczorek discloses the claimed invention except for use of a laser to heat the portions of the material.

A method as claimed in Claim 7, according to which, during step g), said portions of second material are heated using a laser beam.

However, It would have been obvious to one having ordinary skill in the art at the time the invention was made to use the laser since it was known in the art that a laser can be used to anneal a source and/or a drain in order to activate dopants. The use of a laser to anneal a source and drain is disclosed in the abstract of Puchner (U.S. Patent 6358806).

Regarding claim 9. Chau discloses:

A method as claimed in Claim 7, according to which, after step f), encapsulation (420) portions are deposited respectively on top of said portions of second material, on a side opposite to the substrate. (Fig. 4 column 6 lines 1-10, column 7 lines 50-60 column 8 lines 1-10)

Regarding claim 10. Chau in view of Andideh and further in view of Wieczorek does not disclose A method as claimed in Claim 7, according to which step e) is performed before step d).

At the time the invention was made, it would have been an obvious matter of design choice to a person of ordinary skill in the art to perform the steps in the order claimed in claim 10 because Applicant has not disclosed that implementing the steps in this order provides an advantage, is used for a particular purpose, or solves a stated problem. One of ordinary skill in the art, furthermore, would have expected the invention of Chau in view of Andideh and Wieczorek, and applicant's invention, to perform equally well with either the order claimed in claim 7 or the order claimed in claim 10 because both would perform the same function of a semiconductor device, namely a transistor.

Therefore, it would have been prima facie obvious to modify Chau in view of Andideh and further in view of Wieczorek to obtain the invention as specified in claim 10 because such a modification would have been considered a mere design consideration which fails to patentably distinguish over the prior art.

Art Unit: 2822


Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Swapneel Chhaya whose telephone number is 571-270-1434. The examiner can normally be reached on Monday- Thursday 7:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on 571-272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SC


Klesha L. Rose
Primary Examiner
Aug. 20, 2007